Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A probe sheet comprising:

contact terminals arranged in a first surface of the probe sheet to oppose a wafer part to contact with electrodes provided on the wafer part;

wirings, each being drawn from one of ~~said~~the contact terminals in the probe sheet; and

electrode pads, each being arranged in a second surface of the probe sheet at an opposite side thereof to the first surface and electrically connected to one of ~~said~~the wirings,

wherein a pitch between ~~said~~each adjacent electrode pads of the electrode pads in the second surface of the probe sheet is wider than a pitch between ~~said~~each corresponding adjacent contact terminals of the contact terminals in the first surface thereof, and

wherein each of the contact terminals is supported by polyimide.

2. (Currently Amended) ~~The~~A probe sheet according to claim 1,

wherein ~~said~~the contact terminals are arranged according to an array of peripheral electrodes of semiconductor devices formed on ~~said~~the wafer part, and

wherein ~~said~~the electrode pads are arranged in a grid pattern.

3. (Currently Amended) ~~The~~A probe sheet according to claim 1,

wherein a metallic sheet, from which at least a part corresponding to signal electrode pads of the electrode pads is removed, is provided on the second surface of the probe sheet.

4. (Currently Amended) ~~The~~A probe sheet according to claim 3,

wherein a linear expansion coefficient of ~~said~~the metallic sheet is equal to a linear expansion coefficient of ~~said~~the wafer part.

5. (Currently Amended) ~~The~~A probe sheet according to claim 3,

wherein ~~said~~the metallic sheet is a 42 alloy sheet.

6. (Currently Amended) ~~The~~A probe sheet according to claim 1,

wherein dummy terminals, each of which has a larger contact area with the wafer part than that of each of ~~said~~the contact terminals, are provided on the first surface of the probe sheet on which ~~said~~the contact terminals are provided.

7. (Currently Amended) ~~The~~A probe sheet according to claim 1,

wherein ~~said~~the contact terminals are each created by using an anisotropically etched hole in a crystalline substrate as a cast.

8. (Currently Amended) A probe card comprising:

a probe sheet having contact terminals being arranged in a first surface of the probe sheet to oppose a wafer part to contact with electrodes provided on the wafer part, wirings each being drawn from one of the contact terminals, and electrode pads

each being arranged in a second surface of the probe sheet at an opposite side thereof to the first surface and electrically connected to one of ~~said~~the wirings; and

a multi-layer wiring substrate being provided at an opposite side of the probe sheet to the wafer part to face the second surface thereof, the multi-layer wiring substrate has electrodes each being electrically connected to one of ~~said~~the contact terminals through the one of the electrode pads and formed on a surface of the multi-layer wiring substrate, and

wherein a pitch between each adjacent electrode pads of the electrode pads in the second surface of the probe sheet is wider than a pitch between ~~said~~each corresponding adjacent contact terminals of the contact terminals in the first surface thereof, and

wherein each of the contact terminals are supported by polyimide.

9. (Currently Amended) ~~The~~A probe card according to claim 8,

wherein ~~said~~the contact terminals of the probe sheet are arranged according to an array of peripheral electrodes of semiconductor devices formed on the surface of the wafer part, and

wherein the electrodes of ~~said~~the multi-layer wiring substrate are arranged in a grid pattern in the surface thereof.

10. (Currently Amended) ~~The~~A probe card according to claim 8,

wherein the electrodes of ~~said~~the multi-layer wiring substrate are provided in a device-opposed-area on the surface of ~~said~~the multi-layer wiring substrate.

11. (Currently Amended) ~~The~~A probe card according to claim 8,

wherein at least one of capacitors, resistors or fuses are mounted in a device-opposed area on said~~the~~ multi-layer wiring substrate.

12. (Currently Amended) ~~The~~A probe card according to claim 8,

wherein the electrode pads arranged in the second surface of the probe sheet and the electrodes of said~~the~~ multi-layer wiring substrate are electrically connected by a connection part extended vertically with respect said~~the~~ multi-layer wiring substrate.

13. (Currently Amended) ~~The~~A probe card according to claim 8,

wherein the electrodes of said~~the~~ multi-layer wiring substrate are electrically connected to the electrode pads arranged in the second surface of the probe sheet via spring probes disposed therebetween.

14. (Currently Amended) ~~The~~A probe card according to claim 13,

wherein said~~the~~ spring probes are removable.

15. (Currently Amended) ~~The~~A probe card according to claim 8,

wherein each of the electrodes of said~~the~~ multi-layer wiring substrate and each of the electrode pads arranged in the second surface of the ~~problem~~ probe sheet are electrically connected to each other via a wire extended therebetween.

16. (Currently Amended) ~~The~~A probe card according to claim 8,

wherein ~~said~~the probe card ~~has~~is provided with a heating element having a temperature adjustment function.

17. (Currently Amended) ~~The~~A probe card according to claim 8,

wherein ~~said~~the contact terminals are each a pyramid-shaped or truncated-pyramid-shaped terminal created by using an anisotropically etched hole in a crystalline substrate as a cast.

18. (Currently Amended) ~~Semiconductor~~A semiconductor test equipment comprising:

a stage on which a wafer part is mounted; and

a probe card having contact terminals that get in contact with electrodes of semiconductor devices formed on the wafer part and electrically connected to a tester that tests electrical characteristics of the semiconductor devices,

wherein ~~said~~the probe card comprises:

a probe sheet having the contact terminals being arranged in a first surface of the probe sheet opposite to the wafer part, wirings each being drawn from one of the contact terminals, and electrode pads each being arranged in a second surface of the probe sheet at an opposite side thereof to the first surface and electrically connection to one of ~~said~~the wirings; and

a multi-layer wiring substrate whose electrodes electrically connected to the contact terminals via the electrode pads respectively are provided on a surface opposed to the wafer part across the probe sheet, and

wherein a pitch between each adjacent electrode pads of the electrode pads in the second surface of the probe sheet is wider than a pitch between ~~said~~each corresponding adjacent contact terminals of the contact terminals in the first surface thereof, and

wherein each of the contact terminals is supported by polyimide.

19. (Currently Amended) ~~Semiconductor~~A semiconductor test equipment according to claim 18,

wherein a temperature of the stage ~~and the probe card can both be~~is controlled by a heater being provided to the stage and a temperature of the probe card is controlled by a heating element being provided to the probe card.

20. (Currently Amended) ~~The~~A semiconductor test equipment according to claim 18,

wherein ~~said~~the contact terminals are each a pyramid-shaped or truncated-pyramid-shaped terminal created with an anisotropically etched hole in a crystalline substrate as a shape former.

21. (Currently Amended) ~~The~~A probe card according to claim 10,

wherein the device-opposed area is an area of the multi-layer wiring substrate opposite to semiconductor devices formed on the surface of the wafer part across the probe sheet.

22. (Currently Amended) ~~The~~A probe card according to claim 11,

wherein the device-opposed area is an area of the multi-layer wiring substrate opposite to semiconductor devices formed on the surface of the wafer part across the probe sheet, and that at least one of capacitors, resistors or fuses are mounted on a surface of the multi-layer wiring substrate at an opposite side thereof to the wafer part.

23. (Currently Amended) A probe sheet comprising:

contact terminals arranged in a first surface of the probe sheet to oppose a wafer part to contact with electrodes provided on the wafer part;

wirings, each being drawn from one of ~~said~~the contact terminals in the probe sheet; and

electrode pads, each being arranged in a second surface of the probe sheet at an opposite side thereof to the first surface and electrically connected to one of ~~said~~the wirings,

wherein a pitch between ~~said~~each adjacent electrode pads of the electrode pads in the second surface of the probe sheet is wider than a pitch between ~~said~~each corresponding adjacent contact terminals of the contact terminals in the first surface thereof, and wherein ones of ~~said~~the electrode pads extending in a direction away from an area of the contact terminals are laid out in an array having at least three rows extending at least somewhat parallel to the area, and

wherein each of the contact terminals is supported by polyimide.

24. (Previously Presented) A probe sheet as claimed in claim 23, wherein the electrode pads of a subject row of the rows, are staggered with respect to the electrode pads of a neighboring row.

25. (Previously Presented) A probe sheet as claimed in claim 23, wherein the wirings are serpentine wirings, and ones of the serpentine wirings trace serpentine paths between the electrode pads.

26. (Previously Presented) A probe sheet as claimed in claim 25, wherein a pitch between ones of the serpentine wirings varies extending in the direction away from the area of the contact terminals.